

Abstract of the Disclosure:

An integrated memory contains an access controller for controlling an access for the purpose of reading data from, or writing data to, a memory cell array. The access controller
5 accesses the memory cell array in a first double data rate operating mode of the memory in such a manner that a first data item (which is to be written) of an access cycle is written to the memory cell array with a write latency. In a second single data rate operating mode of the memory, the
10 access controller, in contrast, accesses the memory cell array in such a manner that a first data item of an access cycle is, in contrast, written to the memory cell array in an accelerated manner without the write latency of the first operating mode. This makes it possible to read in data values
15 in an accelerated manner in the second operating mode, in particular a test operating mode.

REL/nt